RL4Eng Annual Newsletter - Issue 2

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Introduction about the project

The economic crisis and pandemic in South Mediterranean and sub-Saharan countries have put the HEIs in a challenge to accommodate for the new requirements of online teaching.

The RL4Eng project aims to improve the quality of higher education in third countries and make it more relevant into the today's digital transformation world through establishing Remote and Virtual Laboratories for Teaching and Training Engineering Students to modernize the current teaching approaches and improve the digital and entrepreneurial capacities of both students and teachers in South Mediterranean and Sub-Saharan HEIs.

The project's contribution to the priorities of the call includes the digital transformation under which digital education is the focus of the project. Online teaching for laboratories has been implemented in EU countries with successful outcomes.

The involvement of different European Universities will help integrate good practices and minimise potential risks in implementing the RL4Eng project. South Mediterranean HEIs have identified the necessity of training with numerous initiatives available in the European system. Few Research is available on the effective delivery of remote labs and take-home labs.

The project involves several workpackages in efforts made to elevate the knowledge of remote labs and take home labs in the partners institutions via capacity building for students, staff and faculty and share of experiences.

A remote lab will be established in each country of the partners institutions and a take-home lab will be established in each HEI of the partner countries.

The very nature of remote labs, and take-home labs makes them sustainable and easily scalable as they become part of the university structure and receives part of its budget.

Moreover, the nature of the remote labs makes them sustainable as they are accessible from everywhere and could be used for both teaching and for research.

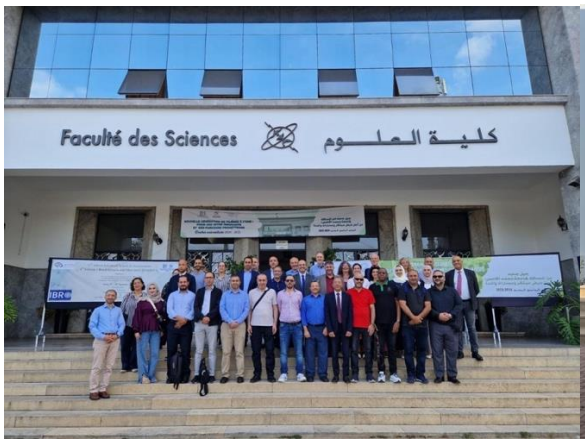
Yarmouk University led the activities and took part in the third meeting of the RL4ENG project held at Mohammed V University in Rabat in Morocco.

Hijjawi College of Engineering Technology at Yarmouk University led the activities and took part in the third meeting of the project " Development of Remote and Virtual Laboratories for Teaching and Training Engineering Students in the South Mediterranean and Sub-Saharan Higher Education Institutions (RL4Eng) which was held at Mohammed V University in Rabat in Morocco.

The RL4ENG project comes within the framework of the ongoing efforts to enhance the role of universities in developing engineering education and training in the Southern Mediterranean and Sub-Saharan region.

The workshops included the participation of 15 partners from Jordan, Lebanon, Morocco, Tanzania, Spain and Germany, with the aim of exchanging knowledge and expertise in the field of engineering education and enhancing the capabilities of faculty members and training students through virtual and remotely managed laboratories.

The project management team at Yarmouk University who took part in the visit included, Dr. Mohammad AlZubaidi, Dean of Hijjawi Faculty for Engineering Technology , Dr. Dania Bani Hani and Dr. Ali Shehade from Hijjawi College of Engineering Technology, presented the university's pioneering role in implementing the project, which demonstrated how faculty members and students at Hijjawi College of Engineering Technology benefit from the resources that the project will provide in the fields of teaching, training and development of graduation projects, which were directed towards vital sectors based on real needs applicable in the local and regional market, with Taking into account technological developments in the field of smart applications.



The project manager, Dr. Mwaffaq Otoom, explained that these initiatives come within the university's efforts to develop the teaching and learning experience, build academic capabilities and enhance applied research through international cooperation and joint projects with academic institutions in various countries of the world, adding that this project represents an opportunity to provide innovative educational models that support students and enable them to engage in developing advanced technological solutions that are in line with the changing needs of the market. He pointed out that Yarmouk University seeks to strengthen its international partnerships and expand the scope of benefiting from such projects to raise the level of engineering education and enhance technological innovation in various fields, with a focus on meeting development needs locally, regionally and globally.

The visit included many sessions which were tailored to reflect on the established remote lab at Mohammed V University in Rabat to demonstrate the lab and its use cases among the students and to exchange some best practices with the other partners as this lab will

be accessible from all partners and worldwide. Several institutional visits were planned as well during the visit to introduce the university and its available labs. Hands on experience was done as well for faculty members to become engaged with the available university labs. Moreover, the visit included some cultural visits to many historical places in Rabat and a traditional food experience was generously provided by the Host. A consortium management meeting was held to reflect on the project progress and plan the way forward.

An example of FPGA Remote Lab Usage at YU “Edge Detection (Sobel Filter)”

Introduction

The FPGA Remote Lab at Yarmouk University provides students with an interactive environment to design and test FPGA-based projects remotely. One of the key tasks implemented in the lab is Edge Detection using the Sobel Filter, which is an essential technique in image processing and computer vision.

This document outlines the key aspects of the Edge Detection experiment, including the theoretical background, design flow, and practical implementation. The objective is to serve as an example of lab utilization and employment, showcasing how students can leverage the remote lab for hands-on learning.

Lab Objective

The primary objectives of the FPGA Remote Lab for **Edge Detection** are:

1. To enable students to compile and upload custom VHDL binary code to an FPGA.
2. To introduce students to edge detection techniques using an FPGA-based remote lab setup.
3. To provide hands-on experience with image processing on an FPGA platform.

Theoretical Background: Edge Detection & Sobel Filter

Edge detection is a fundamental operation in image processing, identifying sharp intensity changes in an image to highlight object boundaries. The Sobel Filter is a widely used technique due to its efficiency in calculating image gradients.

The Sobel operator applies two convolution kernels to an image:

- **Horizontal kernel (Gx)** detects edges in the vertical direction.
- **Vertical kernel (Gy)** detects edges in the horizontal direction.

After applying these filters, the gradient magnitude and direction are computed to highlight the significant edges in the image.

Implementation & Design Flow

1. **Download & Setup:**
   - Students download the provided VHDL source files for the FPGA design.
   - A new project is created in Intel Quartus Prime Lite Edition 23.1.
2. **Adding & Configuring Files:**
   - Import the necessary VHDL files, including lane.vhd, lane_sobel.vhd, and other supporting modules.
   - Configure FPGA settings and specify the correct family and device category.
3. **Compilation & Binary Generation:**
   - The project is compiled, generating a binary (.sof) file required for FPGA programming.
4. **Remote Lab Access:**
   - Students log in to the FPGA Remote Lab at weblab.yu.edu.jo/weblab.
   - The designated experiment is reserved for execution.
5. **Uploading & Running the Experiment:**
   - The FPGA binary file and a test image are uploaded to the remote lab interface.
   - The Sobel filter is applied, detecting the edges in the uploaded image.
6. **Observation & Results:**
   - The output image, with detected edges, is displayed in the lab interface.
   - Students analyze the results to verify the effectiveness of their implementation.

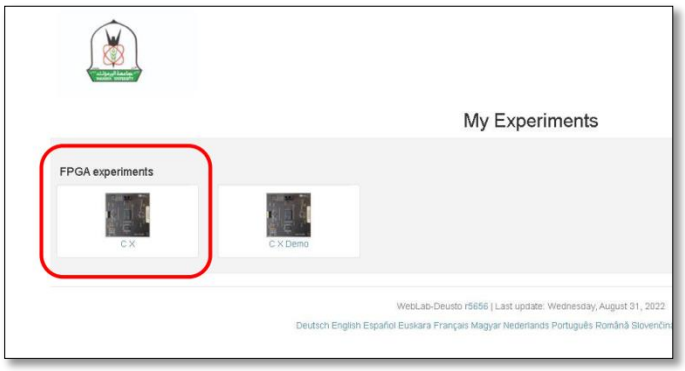
Conclusion & Impact

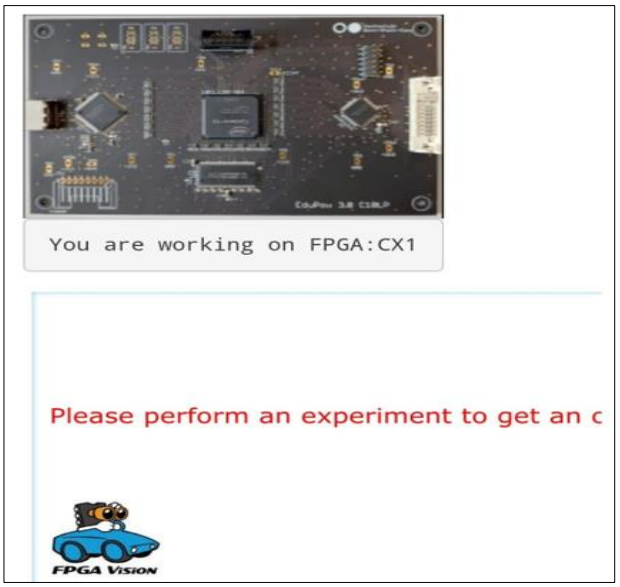
The FPGA Remote Lab provides an invaluable opportunity for students to experiment with hardware design concepts without requiring physical access to FPGA boards. Through this exercise, students gain practical experience with:

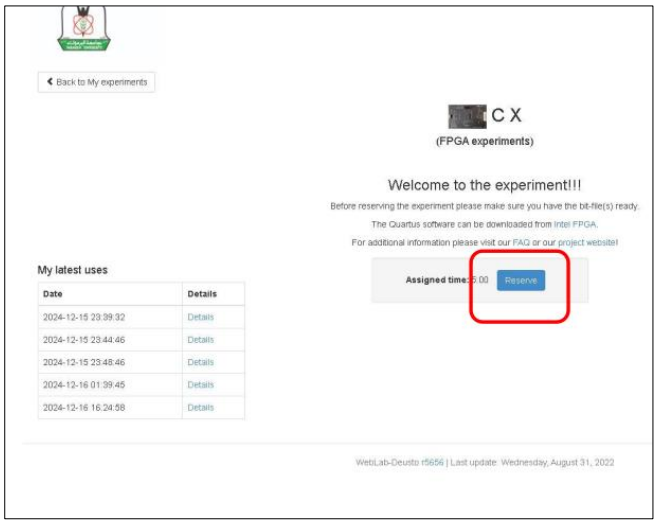
- FPGA programming and synthesis.
- Image processing techniques in hardware.
- Remote experimentation and real-time testing.

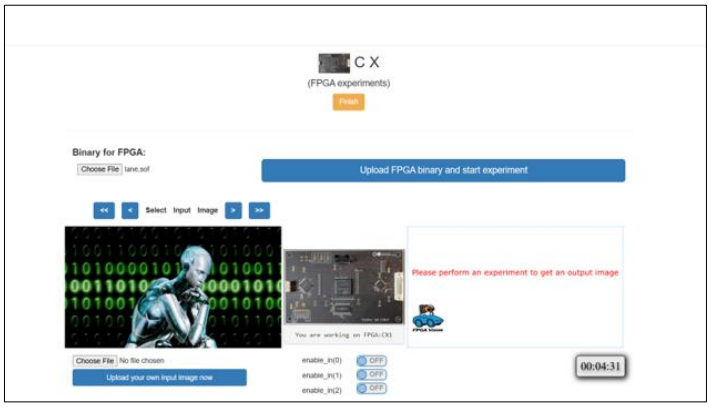
This documented use case can serve as an example for other students and institutions interested in leveraging remote labs for advanced learning.

Images & Visuals









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Department of Computer Engineering

Yarmouk University Remote Lab (FPGA): From Virtual Access to Innovation

Yarmouk University has introduced an **FPGA Remote Lab**, which provides students with a cutting-edge platform to design, implement, and test FPGA-based projects remotely. This Lab eliminates geographical barriers, and grants students hands-on experience with hardware programming from anywhere. Moreover, the remote lab setup allows students to experiment without the need for expensive physical equipment, making high quality education more accessible and cost effective.

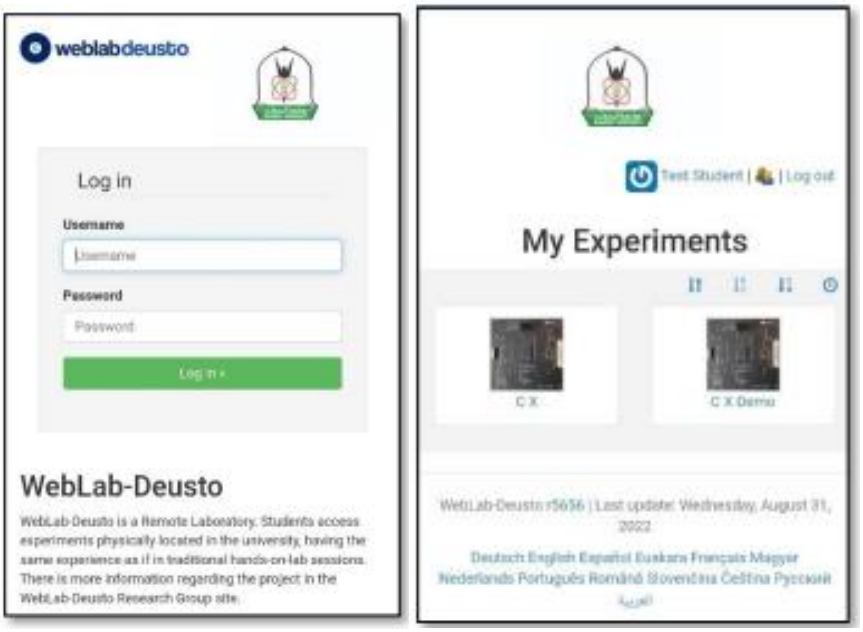
Through a well-defined and user-friendly workflow, students compile and upload their FPGA designs, process images, and analyze real-time results via a remote interface. A wide range of experiments are available, covering various image processing techniques and extending to machine learning applications, allowing students to explore both traditional and AI-driven approaches in FPGA acceleration.

One of the exceptional experiments available in the lab is Edge Detection using the Sobel Filter, which is a fundamental technique in image processing and computer vision. This experiment allows students to explore real-world applications of FPGA technology. Through this experiment, students not only become proficient in FPGA programming but also gain a greater understanding of how digital hardware can enhance processing speed and efficiency in complex algorithms.

By bridging theoretical knowledge and practical experience, the FPGA Remote Lab is transforming engineering education. Students gain essential skills in FPGA programming, Preparing them for careers in embedded systems, AI acceleration, and advanced hardware design.

The remarkable success of YURL showcases its positive impact on education. It serves as a model for institutions worldwide by demonstrating how remote labs can significantly enhance and support advanced learning in engineering disciplines.

Ameera Almomani
Computer Engineer, YU
YURL Administrator


weblabdeusto
Log in
Username
Password
Log in »
WebLab-Deusto
WebLab-Deusto is a Remote Laboratory. Students access experiments physically located in the university, having the same experience as if in traditional hands-on lab sessions. There is more information regarding the project in the WebLab-Deusto Research Group site.
Test Student | | Log out
My Experiments
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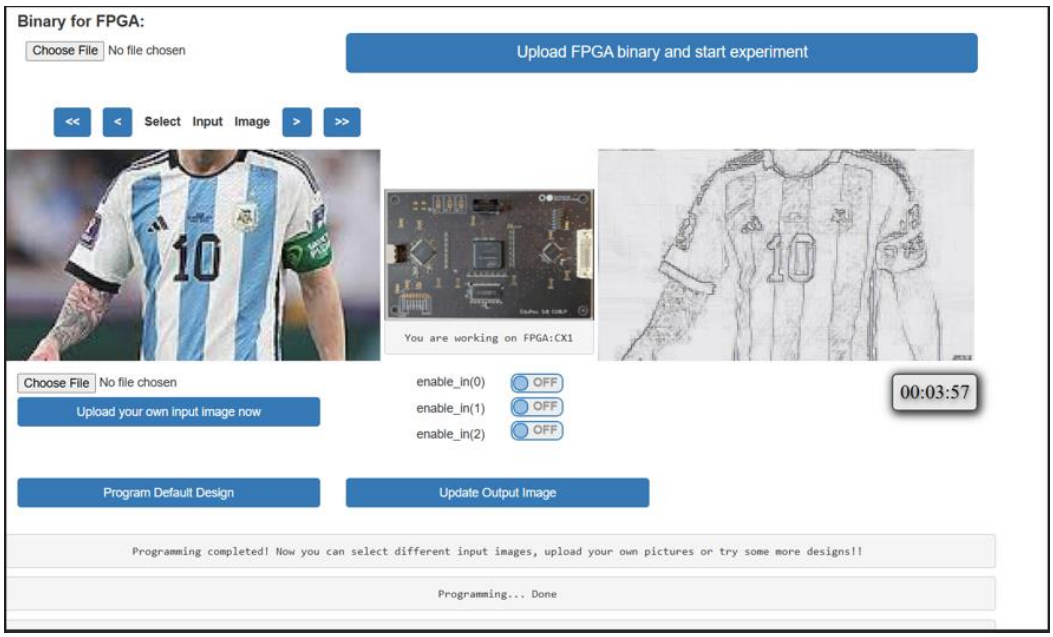
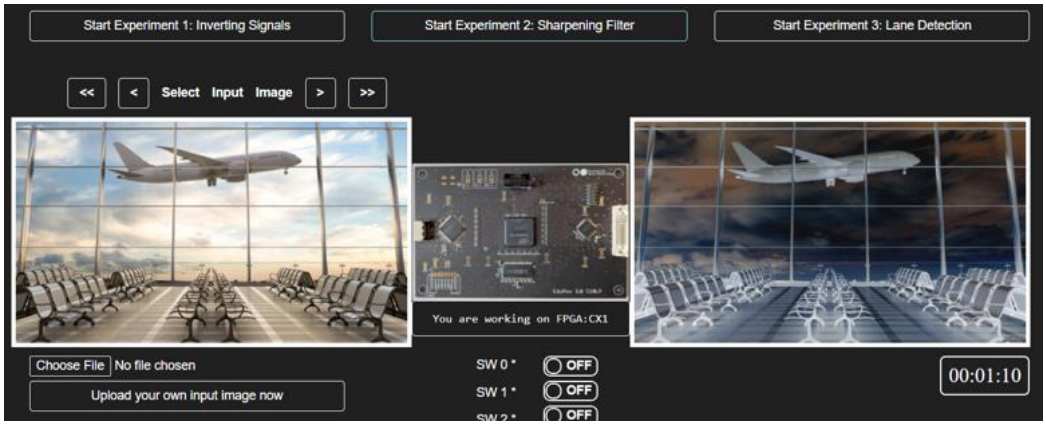
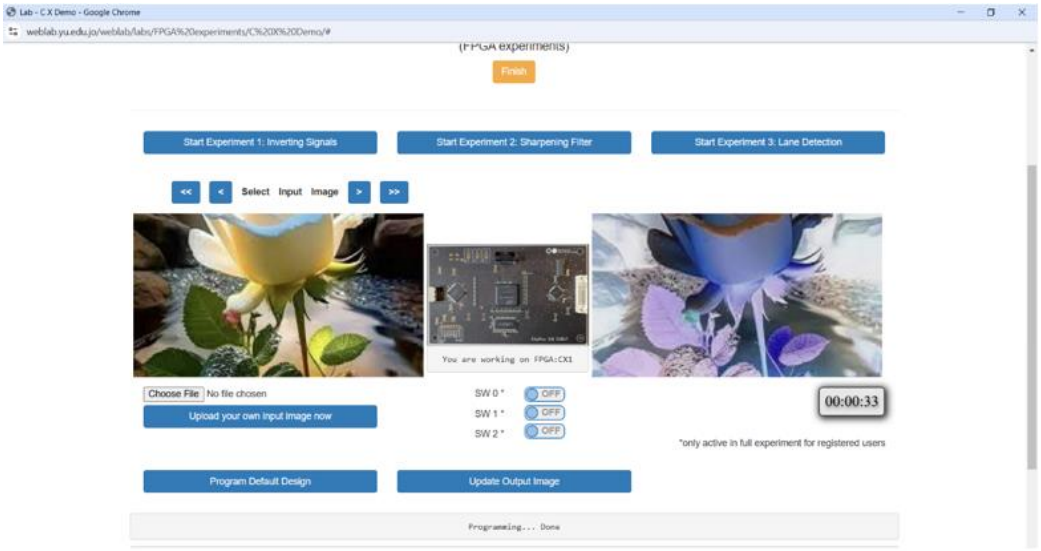
C X Demo
WebLab-Deusto r5636 | Last update: Wednesday, August 31, 2022
Deutsch English Español Euskara Français Magyar Nederlands Português Română Slovenčina Čeština Русский


Binary for FPGA:
Choose File No file chosen
Upload FPGA binary and start experiment
<< < Select Input Image > >>
You are working on FPGA:CX1
Choose File No file chosen
Upload your own input image now
enable_in(0) OFF
enable_in(1) OFF
enable_in(2) OFF
00:03:57
Program Default Design
Update Output Image
Programming completed! Now you can select different input images, upload your own pictures or try some more designs!!
Programming... Done






```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.NUMERIC_STD.all;

entity lane is
  port (clk        : in  std_logic;                     -- input clock 74.25 MHz, video 720p
        reset_n    : in  std_logic;                     -- reset (invoked during configuration)
        enable_in : in  std_logic_vector(2 downto 0);   -- three slide switches
        -- video in
        vs_in      : in  std_logic;                     -- vertical sync
        hs_in      : in  std_logic;                     -- horizontal sync
        de_in      : in  std_logic;                     -- data enable is '1' for valid pixel
        r_in       : in  std_logic_vector(7 downto 0);  -- red component of pixel
        g_in       : in  std_logic_vector(7 downto 0);  -- green component of pixel
        b_in       : in  std_logic_vector(7 downto 0);  -- blue component of pixel
        -- video out
        vs_out     : out std_logic;                     -- corresponding to video-in
        hs_out     : out std_logic;
        de_out     : out std_logic;
        r_out      : out std_logic_vector(7 downto 0);
        g_out      : out std_logic_vector(7 downto 0);
        b_out      : out std_logic_vector(7 downto 0);
        --
        clk_o      : out std_logic;                     -- output clock (do not modify)
        led        : out std_logic_vector(2 downto 0));  -- not supported by remote lab
end lane;
```

Second THL workshop at the Faculty of Engineering of the Lebanese University

Within RL4ENG project activities, a second workshop is achieved on March 27, 2025 at the Faculty of Engineering for the students (third year of Electrical and electronics Engineering, spring semester). The concepts of the remote labs and take-home labs are presented and discussed with the students. A local training focusing on Arduino installation, features and programming is done. Then the LUTHL4EEE kits are distributed to the students and they are invited to conduct the RL4ENG Pre-Survey for Take Home Labs.

RL4eng

Partners







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